EECS 427 CAD GRADING SHEET Winter 2023

**CAD9** Name: **\_\_\_\_Group 7\_\_\_\_\_**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | Cell | Item | Credit | | |
| Complete | Baseline | Schematic | 1 | / | 1 |
| Layout | 1 | / | 1 |
| Speed | 2 | / | 3 |
| Assembly Program | 1 | / | 1 |
| NCVerilog One Cycle Correctness | 3.5 | / | 4 |
| DRC/LVS | 2 | / | 2 |
| Pipelined | 1 | / | 1 |
| Project | Correct Waveforms | 1 | / | 2 |
| DRC/LVS | 2 | / | 2 |
| Quality (Design Considerations, Difficulty) | 1.5 | / | 5 |
| Co-simulation with baseline | 0 | / | 2 |
| Total | | 16 | / | 24 |
| Quality | Area Efficiency | | 1.5 | / | 3 |
| Clock Tree | | 1 | / | 1 |
| Power Routing/Rings/Stripes | | 1 | / | 1 |
| Off-chip Inputs | | 0.5 | / | 1 |
| Total | | 4 | / | 6 |

**Total Score**: 20 / 30

**Timestamp**: 4/20/2023

**Comments:**

+ Organized presentation

+ Good illustration for clk tree

+ Power routing is good for the core

- Floorplan can be further optimized

- Okay baseline clock speed

- Fibonacci calculation not optimal for registers

- Scope of the project is small

- Needs a NOR for SRAM Boolean calculation, not optimal for instruction per cycle, output is not hold for the entire 2-cycle

- Missing baseline co-simulation

- Limited simulation results, lacking enough analog simulation results

- Missing explanation for off-chip inputs/pads